IN THE SPECIFICATION

Please amend the specification as follows. Paragraphs that are being amended are listed in their entirety; changes are indicated in the left margin with a vertical change bar. Deletions are marked by ~~strikethrough~~; insertions are underlined.

Please amend the paragraphs beginning on page 3, line 17, through page 4, line 20, as follows:

The effects of overlay error are typically divided into the following two major categories for the purpose of quantifying overlay error and making precise exposure adjustments to correct the problem. The first category, grid or inter-field error, is the positional shift and rotation or yaw of each exposure pattern, exposure field, or simply field, with reference to the nominal center position of the wafer 2001 and 2010 in Figures ~~20 and 20A~~ 20A and 20B, respectively.

Referring to Figure ~~20~~ 20A, the intra-field error in field placement on the wafer is shown as a vector offset 2002 for each field. This vector offset is the difference in the placement of the field center from its ideal or nominal position and actual position, and represents one of the components of the inter-field error, that the present invention will determine. Figure ~~20A~~ 20B shows the other part of intra-field error, which is the yaw or rotational error in the placement of the individual fields, that is also determined by this technique.

Overlay modeling algorithms typically divide grid or inter-field error into sub-categories or ~~components~~ components, the first five of which are translation, rotation, magnification or scale, non-orthogonality, and stage distortion. *See* Matching Performance for Multiple Wafer Steppers Using an Advanced Metrology Procedure, *supra*. The following discussion is concerned with wafer stage distortion and yaw induced registration or overlay ~~error~~ error; these global or inter-field positional errors may be caused by the wafer stage subsystem of the stepper.

The second category, intra-field overlay error, is the positional offset of an

individual point inside a projected field referenced to the nominal center of an individual exposure field, as illustrated in Figure ~~20~~ 20A. Here the term "nominal center" means the exact location of the center of a perfectly aligned exposure field. Figure ~~20~~ 20A schematically shows intra-field overlay error as a set of vector displacements within the exposure field, each vector representing the magnitude and direction of the placement error. The following four main components each named for a particular effect are typically used to describe the sources of intra-field error: translation, rotation, scale or magnification, and lens distortion.

Please amend the paragraph beginning on page 7, line 10, through page 8, line 4, as follows:

Several common procedures are used to determine the relative magnitude of wafer stage placement error, semi-independent of other sources of registration or overlay error. Semiconductor manufacturing facilities use the resulting placement error information to manually or automatically adjust the wafer stage and stepper alignment system in such a way as to minimize the impact of overlay error. The technique has been simplified for illustration. *See* Matching Management of Multiple Wafer Steppers Using a Stable Standard and a Matching Simulator, *supra*; Matching Performance for Multiple Wafer Steppers Using an Advanced Metrology Procedure, *supra*. Figure 3 shows a typical set of geometrically placed overlay target patterns consisting of a matching pair of male 302 and female 304 targets. The male 302 and female 304 targets are regularly spaced across a wafer stage test reticle 306 as shown in Figure 3. It should be noted that the chrome target patterns on most reticles are 4 or 5 times larger as compared with the patterns they produce at the image ~~plane~~ plane; this simply means modern steppers or projection lithography tools are reduction systems. First, a photoresist coated wafer is loaded onto an exposure tool or stepper wafer stage and globally aligned. Next, the full-field image of the wafer stage test reticle is exposed several times at various positions across the surface of the photoresist coated wafer, see Figure 22. In addition, several

wafer alignment marks are also printed across the wafer using the wafer stage test reticle as shown in Figures 3 and 22. For purposes of illustration, we assume that the full-field of the wafer stage test reticle consists of an 11-by-11 array of male and female target pairs (separation d*M) evenly spaced at pitch p'*M, across the reticle surface, see Figures 3 and 5. The pattern is then sent through the remaining portions of the lithographic patterning process to delineate the resist pattern.

Please amend the paragraph beginning on page 9, lines 1-6, as follows:

An important point is that the resulting inter-field or wafer stage overlay error does not yield the unique overlay error of the wafer stage in ~~question, instead~~ <u>question; instead,</u> it only can be used to report the inter-field or wafer stage overlay error as referenced to another machine stage, sometimes called a "mother" or "reference machine". In general, semiconductor manufacturers rely on some kind of stage matching or cross-referencing technique to calculate the relative wafer stage overlay error.

Please amend the paragraphs beginning on page 12, line 4, through page 16, line 19, as follows:

Problems with this technique are: the systematic (repeatable) and random grid errors on the reference machine (the machine used for creating the reference wafers) are permanently recorded as half (inner or outer box) of our factory wide metrology standard. The magnitude and distribution of these errors is entirely unknown. For machine to machine comparisons of grid errors, the systematic or repeatable parts of the errors cancel ~~out~~ <u>out,</u> but the influence of the random or non-repeatable error remains. This is why multiple reference wafers are typically used to improve machine to machine matching ~~results *See*~~ <u>results. *See*</u> Matching Management of Multiple Wafer Steppers Using a Stable Standard and a Matching Simulator, *supra*. Furthermore, reference machine instabilities over time lead to a drift or error in the factory wide standard represented by the reference machine. Yet

another problem with this technique is that because it utilizes full size projected fields to determine the inter-field errors, it does not work with partially exposed fields as illustrated in Figure 44. The ability to include partially exposed fields is important since product wafers typically contain multiple die within an exposure ~~field~~ field, and therefore the inter-field error of partially exposed fields is important since it directly affects the edge die overlay error.

Another technique for grid error determination utilizing self-calibration is discussed in *See* Self-calibration in Two-Dimensions: The Experiment, M. Takac, J. Ye, M. Raugh, R. Pease, C. Berglund, G. Owen, SPIE Vol. 2725, 130:146, 1996; Error Estimation for Lattice Methods of Stage Self-calibration, M. Raugh, SPIE. Vol. 3050, 614:625, 1997. It consists of placing a plate (artifact) with a rectangular array of measurable targets on a tool stage and measuring the absolute positions of the targets using the tool's stage and the tool's image acquisition or alignment system. This measurement process is repeated by reinserting the artifact on the stage but shifted by one target spacing in the X direction, then repeated again with the artifact inserted on the stage shifted by one target spacing in the Y direction. Finally, the artifact is inserted at 90 degrees relative to ~~it's~~ its initial orientation and the target positions measured. The resulting tool measurements are a set of (x, y) absolute positions in the tool's nominal coordinate system.

Using the technique described in Self-calibration in Two-Dimensions: The Experiment, *supra*; and Error Estimation for Lattice Methods of Stage Self-calibration, *supra*, the absolute position of both targets on the artifact and a mixture of the repeatable and non-repeatable parts of the stage x,y grid error are then determined to within a global translation (Txg, Tyg), rotation (qg) and overall scale ((sxg+syg)/2) factor. Unfortunately, this technique cannot be applied to photolithographic exposure tools (machines) since the wafer position (artifact) typically cannot be placed on the wafer chuck in a position significantly (>= 1mm) shifted from the nominal position. In some machines, such a shift may be possible with extraordinary effort on the part of the maintenance engineer, but such a

procedure is completely unsuitable in ordinary production use. Wafers (artifacts) can typically be automatically reinserted on the wafer chuck rotated 90 degrees from nominal, but without the additional X or Y shifts described above, the resulting reconstructed grid errors are missing all of the 4-fold symmetric grid distortions. *See* Self-calibration in Two-Dimensions: The Experiment, *supra;* Error Estimation for Lattice Methods of Stage Self-calibration, *supra*. Another disadvantage of this technique is that it does not measure the stage yaw. While this is not necessary for absolute metrology tools that measure target positions over relatively small optical fields (<0.5mm) such as the Nikon ~~5I. *See*~~ 5I (*See* Measuring System XY-5i, K. Kodama, et. al., SPIE Vol. 2439, 144:155, 1995 or the Leica LMS IPRO Brochure, ~~Leica,~~ Leica), it is absolutely essential for production machines running at large projection fields (> 10mm) such as the Nikon S205. *See* Nikon Lithography Tool Brochures (Japanese), Nikon. Yet another disadvantage of the aforementioned technique is that the measurement process utilizes the production machine itself to perform the ~~metrology,~~ metrology; this means there is less time available for making product on that machine. Yet another disadvantage of this technique is it does not allow us to measure stage error for partially exposed fields.

~~Therefore~~ Therefore, there is a need for overlay metrology tool to determine wafer stage positional errors. In addition, there is a need to measure the wafer stage positioned error in a production environment by the day to day operating personnel. There is also a need to determine the inter-field error of partially exposed fields.

SUMMARY OF THE INVENTION

A wafer stage error map is created using standard overlay targets and a special numerical algorithm. A reticle consisting of a 2-dimensional array of standard overlay targets is exposed several times onto a photoresist coated silicon wafer using a photolithographic projection tool (machine). Next, the overlay targets are measured for placement error using a conventional overlay metrology tool. The

resulting overlay error data ~~is~~ are then fed into a software program that generates a 2-dimensional wafer stage error map. Most importantly, the method determines wafer stage overlay error, namely, wafer stage distortion and yaw, excluding, total or average translation, and rotation. In summary, the projected field of the overlay reticle is used as a rigid 2-dimensional ~~ruler~~ ruler, and the stage errors are determined in detail with respect to the dimensions of a single projected image field. The method described above does not require the use of a special reference stepper or golden wafer to obtain the wafer stage contributions to placement error. The preferred embodiment is both self-consistent and self-referenced thus reducing the need of cross calibration between different exposure tool sets to a bare minimum. In addition, variations of the preferred embodiment can be used to calculate stage repeatability or precision using standard statistical methods. The ability to determine true stage distortion and yaw without cross calibration or reference to other stepper systems allows the user to more accurately model additional sources of placement error. The method described above can be adjusted for accuracy by simply adjusting the number of measurements made of the alignment attributes or overlay targets. The invention requires exposing and printing an array of fields in a periodic interlocking pattern across the wafer. Next, the resulting overlay target patterns can be measured for overlay error using a standard commercially available optical overlay metrology tool. Next, the distortion and yaw components of stage overlay error are computed using a special algorithm. The method and apparatus form a methodology that can be modified slightly to achieve varying degrees of overall accuracy. The following procedure can be easily implemented in a modern semiconductor manufacturing facility.

A reticle containing special overlay target patterns, for example, see Figure ~~21~~ 21A, is placed into a projection imaging tool or machine, as shown in ~~Figure 19. Where~~ Figure 19, where the term lithographic exposure tool includes contact or proximity printers, steppers, scanners, direct write, e-beam, x-ray, SCALPEL, IPL, or EUV machines. *See* Direct-referencing Automatic Two-Points Reticle-to-Wafer

Alignment Using a Projection Column Servo System; M. Van den Brink, H. Linders, S. Wittekoek, SPIE Vol 633, Optical Microlithography V, 60:71, 1986; New 0.54 Aperture I-Line Wafer Stepper with Field by Field Leveling Combined with Global Alignment, M. Van den Brink et al., SPIE Vol. 1463, 709:724, 1991; US Patent 4,861,146, entitled Variable Focal Lens Device, Hatase et al., August 29, 1989. Micrascan(TM) III Performance of a Third Generation, Catadioptric Step and Scan Lithographic Tool, D. Cote, et. al., SPIE. Vol. 3051, 806:816, 1997; ArF Step And Scan Exposure System For 0.15 Micron and 0.13 micron Technology Node, *supra*; 0.7 NA DUV Step and Scan System for 150nm Imaging with Improved Overlay, *supra*; Optical Lithography - Thirty Years and Three Orders of Magnitude, J. Bruning, SPIE Vol. 3051, 14:27, 1997; Large Area Fine Line Patterning By Scanning Projection Lithography, H. Muller, et. al., MCM 1994 Proceedings, 100:104; US Patent 5,285,236 entitled Large-area, High-throughput, High-Resolution Projection Imaging System, K. Jain, February 8, 1994; Development of XUV Projection Lithography at 60-80 nm, B. Newnam, et. al., SPIE vol. 1671, 419:436, 1992; Mix-And-Match: A necessary Choice, *supra*; Optical Lithography - Thirty Years and Three Orders of Magnitude, *supra*. Next, a photoresist coated wafer is loaded onto the machine; fine wafer alignment is unnecessary.

A series of projection field exposures each containing a sub-array of overlay target patterns is exposed onto the photoresist coated wafers in a partially overlapping interlocking pattern as illustrated in Figures 13, ~~14~~ 14A, ~~14A~~ 14B, and 26. Each projection field exposure is separated from the previous exposure by a distance such that neighboring fields will have the inner or outer boxes closest to their perimeters interlocking from one field to another, as shown in Figure ~~14A~~ 14B. After the final exposure the wafer is removed from the machine and sent through the final resist development steps.

Please amend the paragraphs beginning on page 18, lines 8-9, as follows:

Figure ~~8~~ 8A shows outer box 2 as printed on wafer;

Figure ~~8A~~ 8B shows outer box 2 on the reticle, M=4;

Please amend the paragraphs beginning on page 18, lines 11-12, as follows:

Figure ~~10~~ 10A shows inner box 1 as printed on wafer;

Figure ~~10A~~ 10B shows inner box 1 on the reticle, M=4;

Please amend the paragraphs beginning on page 18, lines 14-16, as follows:

Figure ~~12~~ 12A shows a typical overlay reticle overlay set or group as projected onto a wafer;

Figure ~~12A~~ 12B shows a completed alignment attribute;

Please amend the paragraphs beginning on page 18, lines 19-21, as follows:

Figure ~~14~~ 14A shows overlay target patterns in the y-direction creating interlocking rows;

Figure ~~14A~~ 14B shows an interlocking exposure of 4 adjacent fields;

Please amend the paragraphs beginning on page 19, lines 4-7, as follows:

Figure ~~20~~ 20A shows examples of inter-field and intra-field overlay error;

Figure ~~20A~~ 20B shows an example of inter-field yaw error;

Figure ~~21~~ 21A shows the preferred embodiment overlay reticle in plan view;

Figure 21B shows a side view of the reticle of Figure ~~21~~ 21A;

Please amend the paragraphs beginning on page 20, line 14, through page 21, line 20, as follows:

DETAILED DESCRIPTION

We are concerned here with measuring the wafer stage-induced overlay error, sometimes called grid or inter-field error. In order to measure and quantify the

overlay error that exists between device ~~layers~~ layers, special overlay target patterns are printed in special locations across the wafer at each lithographic processing step. If the two patterned layers are perfectly aligned to each ~~other~~ other, the overlay target patterns will form a perfectly centered box-in-box or frame-in-frame target pattern, as illustrated in Figure 31. If the two patterned layers are not perfectly ~~aligned in a~~ aligned, the box-in-box pattern will not be perfectly aligned, for example see Figure 30. The positional offset or ~~misalignment,~~ misalignment of the box-in-box target pattern is a measure of the overlay error. Figure 1 shows a variety of different overlay target patterns or completed alignment attributes ready to be measured for overlay error. The positional offset of the box-in-box overlay target pattern is measured with a commercial optical overlay metrology tool. In some cases, the overlay error can be measured using the photolithographic exposure tool's alignment system. *See* Matching Management of Multiple Wafer Steppers Using a Stable Standard and a Matching Simulator, *supra*. Vector displacement plots as shown in Figures 27-29, give a visual description of the ~~direction,~~ direction and magnitude of overlay error that are mathematically separated into different spatial components using a variety of regression routines. Many commercial software packages exist (Monolith A Computer Aided Engineering Workstation for Registration Control, *supra*, Klass II Lens Matching and Distortion Testing in a Multi-Stepper, Sub-Micron Environment, *supra*) that model and statistically determine the intra-field error components for the purpose of process control and exposure tool set-up. Once determined, they are analyzed and used to adjust the calibration constants of the wafer handling stage to improve pattern alignment. In addition, since different exposure tools are used to produce a given device the exposure tools must be matched or fingerprinted and adjusted so that registration errors unique to one tool are removed or minimized as much as possible. *See* Mix-And-Match: A Necessary Choice, *supra*.

We now describe a simple and accurate methodology that allows for the extraction of the components of wafer stage overlay error, namely wafer stage distortion and yaw effects excluding total ~~translation,~~ translation and rotation, see Figure 18. In what follows, machine refers to the projection imaging tool whose wafer or substrate stage is being measured.

Please amend the paragraphs beginning on page 22, line 1, through page 24, line 3, as follows:

Reticle

A reticle, the preferred embodiment is shown in Figure ~~21~~ 21A, containing an Mx by My array of overlay groups is provided. Dimensions on the preferred embodiment of the reticle are designated as multiples of the reduction magnification ratio M (typically 4 or 5) of the machine on which the reticle is to be typically used. This means that dimensions as projected onto the wafer will be M times smaller than the reticle dimensions. The overlay groups on pitch M*p each consist of three features or alignment attributes each, two of which are distinct and labeled 1 and 2 in Figure ~~21~~ 21A, shown schematically as two small boxes and a large box with an X through it. Alignment attributes 1 and 2 form a complementary ~~pair,~~ pair; when combined by projecting and overlaying them one upon another they form a completed, readable alignment attribute, examples of which are shown in Figure 1 and in more detail in Figure ~~12A~~ 12B. Alignment attributes or features 1 are offset in distinct orthogonal directions from feature 2 by a distance M*dp. Figures ~~8 and 10~~ 8A and 10A show particular examples of features 2 and 1 respectively as projected onto a wafer and printed in positive photoresist, while Figure ~~12~~ 12A shows an overlay group consisting of the projected features of Figures ~~8 and 10~~ 8A and 10A.

Referring to Figures 7, 9, 11, and ~~21~~ 21A, the dimension M*p that determines the pitch will typically be in the range of about 2mm to about 35mm. The upper limit on the pitch M*p is set by the need to have at least two rows and columns of overlay groups present on the projected field and that the interlocking rows and columns

have at least two (2) useable, completed alignment attributes. Referring to Figure ~~14A~~ 14B, the completed alignment attribute ~~become~~ becomes unusable, labeled UA in Figure ~~14A~~ 14B, when more than two (2) distinct fields overlap to create the alignment attribute. Completed alignment attribute UA is not useable since it is created by the overlap of three (3) distinct fields, while the completed alignment attributes labeled CA in Figure ~~14A~~ 14B are useable since they are the result of only two (2) overlapped fields. Thus, if the projected field of the machine has (x,y) dimensions of ~~(Wx, Wy)~~ (Wx, Wy), then for the reticle of Figure ~~21~~ 21A to be useable on this machine we must have at least two useable alignment attributes between adjacent ~~fields,~~ fields; this means:

$$p < \min(Wx-dp, Wy-dp)/4 \qquad \text{(eq 5.5)}$$

where min(a,b) is the minimum of the numbers a and b.

An aspect of the reticle is that it be capable of creating interlocking rows and columns of completed alignment attributes in a periodic array when exposed for at least one choice of the field stepping pattern. Figure ~~14A~~ 14B shows an example of a reticle of the type shown in Figure ~~21~~ 21A exposing an Nx X Ny = 4 x 4 array with a field stepping pattern of (Fx, Fy) = (3*p+dp, 3*p+dp). Here, (Fx, Fy) are the (x,y) field stepping distances on the wafer. The interlocking rows and columns of the resulting pattern at the wafer are indicated. Within the interlocking rows and columns, some of the completed alignment attributes (CA) are indicated. The reticle, once provided, is loaded into the machine's reticle handling system, loaded into the exposure position and aligned.

Exposure

Next, a photoresist coated wafer is loaded onto the wafer stage of the machine (shown schematically in Figure 19). A series of field exposures each containing an Nx by Ny
(Nx <= Mx, Ny <= My) array of overlay groups is exposed onto the photoresist coated wafer in an interlocking pattern, see Figures ~~14A~~ 14B and 26, producing

interlocking rows and columns containing completed alignment attributes. For the reticle of Figure ~~21~~ 21A, following the first exposure, subsequent exposures in the same row are separated by a distance of Fx = (Nx-1)*p + dp or the distance between the leftmost outer box of the projected field and the rightmost inner box of the projected field. Subsequent exposures in the same column are separated by a distance of Fy = (Ny-1)*p + dp or the distance between the outer box at the bottom of the projected field and the topmost inner box within the projected field, as shown in Figure ~~21~~ 21A.

Please amend the paragraphs beginning on page 24, line 18, through page 25, line 18, as follows:

Develop and Measure

After the last exposure is complete, the wafer is removed from the wafer stage and sent through the final few resist development steps. The resulting overlay target patterns or box-in-box structures are then measured for registration, placement or overlay error using an overlay metrology tool such as a KLA-Tencor model 5100. *See* KLA 5105 Overlay Brochure, *supra*; KLA 5200 Overlay Brochure, *supra*. For each full exposed field, we measure at least two completed alignment attributes along each interlocking edge (row or column) with the adjacent full exposed field. For partially exposed fields, we need to measure at least two completed alignment attributes along all of ~~its'~~ its interlocking edges. The resulting overlay data set is entered into a computer algorithm for ~~analysis~~ analysis, and the overlay components associated with wafer stage distortion and stage yaw are calculated. If desired, the resulting data can be plotted to form a wafer stage distortion map. Furthermore, the wafer stage distortion results can be used as input into traditional overlay models to produce more accurate results or used in process control strategies. *See* US Patent 5,877,861, *supra*.

Intra-Field Distortion

At this point the intra-field distortion is provided.

A number of techniques are available for the determination of the intra-field distortion (dxf, dyf). The preferred technique is the method of Smith, McArthur, and Hunter ("Method And Apparatus For Self-Referenced Projection Lens Distortion Mapping", U.S. patent application serial No. ~~60/254,271,~~ 60/254,271), which is a self referencing technique that can be carried out using overlay metrology tools widely available in semiconductor factories and allows for highly accurate determination of the intra-field distortion (dxf, dyf) over a set of grid points to within an x, y translation, rotation, and overall scale or symmetric magnification factor.

Please amend the paragraph beginning on page 26, line 14, through page 27, line 8, as follows:

Compute Stage Errors

The following model is used in the determination of the stage errors:

BBx(i,j;a,T) = [dxG(i,j+1) + dxf(a,B) – Qg(i,j+1)*yfn(B)] – [dxG(i,j) + dxf(a,T) – Qg(i,j)*yfn(T)]
= dxG(i,j+1) – dxG(i,j) - Qg(i,j+1)*yfn(B) + Qg(i,j)*yfn(T) + dxf(a,B) - dxf(a,T) (eq 6)

BBy(i,j;a,T) = [dyG(i,j+1) + dyf(a,B) + Qg(i,j+1)*xfn(a)] – [dyG(i,j) + dyf(a,T) + Qg(i,j)*xfn(a)]
= dyG(i,j+1) – dyG(i,j) + Qg(i,j+1)* xfn(a)- Qg(i,j)*xfn(a) + dyf(a,B) - dyf(a,T) (eq 7)

BBx(i,j;b,R) = [dxG(i+1,j) + dxf(b,L) – Qg(i+1,j)*yfn(b)] – [dxG(i,j) + dxf(b,R) – Qg(i,j)*yfn(b)]
= dxG(i+1,j) – dxG(i,j) - Qg(i+1,j)*yfn(b) + Qg(i,j)*yfn(b) + dxf(b,L) - dxf(b,R) (eq

8)

BBy(i,j;b,R) = [dyG(i+1,j) + dyf(b,L) + Qg(i+1,j)*xfn(L)] – [dyG(i,j) + dyf(b,R) + Qg(i,j)*xfn(R)]
= dyG(i+1,j) – dyG(i,j) + Qg(i+1,j)*xfn(L) - Qg(i,j)*xfn(R) + dyf(b,L) - dyf(b,R) (eq 9)

~~Where;~~ Where:

T, B, R, L = designate the top, bottom, right and left most row or column within each field, see Figure 40.

Please amend the paragraphs on page 32, lines 4-24, as follows:

Further Interpretation of the Solution For Intra-field Error

General

What the above procedure accomplishes is a detailed assessment or map of the wafer stage distortion (dxG(i,j), dyG(i,j)) and yaw (Qg(i,j)), both called stage error for short. This map will contain both systematic and random components. By systematic, we mean that there is a portion of (dxG, dyG, Qg) (i,j) that will be constant or unvarying over a short (< 1 day) period of ~~time~~ time, and by random components we mean that portion of (dxG, dyG, Qg)(i,j) which varies over a short time period. By measuring the stage error using a number of wafers over a short time period, we can apply standard statistical methods to calculate the systematic part of the stage error.

Typically, we will average the results of all the wafers to get the systematic part of the stage error and then characterize the random part in terms of the standard deviation of the resulting distribution of stage error. The systematic part can then be ~~analyzed~~ analyzed, and the stage motion corrected either through lookup corrections to the stage motion, hardware adjustments or a combination of both. Having thereby minimized the stage error as much as possible, the remaining systematic error, which will be the above measured systematic error minus the effect of any corrective action we might have ~~taken~~ taken, and the random error ultimately

determine the best possible performance of the wafer stage. Furthermore, a large or out of machine specification random error should also trigger a wafer stage maintenance to bring the machine back into specification or into the factory wide operating envelope.

Please amend the paragraph beginning on page 36, line 23, through page 37, line 14, as follows:

First, the overlay target reticle and photoresist coated wafer are loaded into the projection lithography tool (machine) and properly aligned as described in the preferred embodiment. Next, the machine is programmed to the same field stepping pattern as used in the preferred ~~embodiment,~~ embodiment; however, in this variation the exposure dose energy for each exposure will be 2*Eo/N, where N is some predetermined number (typically 20) and Eo is the E-zero or minimum exposure dose required for a large (> 200 micron) open area pattern on the reticle to become fully developed or cleared (in the case of positive resist). After the wafer is exposed, the wafer stage is moved back to the first exposure field of the field stepping ~~pattern~~ pattern, and the sub Eo exposure sequence begins again for the second time. This process is repeated N times such that each field in the field stepping pattern will be exposed with a total dose of 2*Eo. The wafer is then removed from the wafer stage and sent on for final resist processing. The finished wafer is then sent for overlay measurement as described in the preferred embodiment. The result of this procedure is to produce a single wafer wherein the random part of the stage error will be effectively averaged out over approximately N/2 or more exposures and thereby minimized with respect to the systematic error resulting in a better estimate of the systematic error than could be obtained with a single wafer and single exposure sequence.

Please amend the paragraph beginning on page 37, line 23, through page 38, line 6, as follows:

<u>2nd Alternate Embodiment</u>

In this embodiment, see flow diagram Figure 17, we also perform multiple exposure sequences to average out the effect of machine random stage ~~error~~ <u>error,</u> but now we provide the overlay reticle of Figure ~~21~~ <u>21A</u> with a partially reflecting dielectric coating either on ~~it's~~ <u>its</u> top (non-chrome) or possibly bottom surface (chrome coated or machine optical object plane), as shown in Figure 21B. A 95% reflecting dielectric coating applied to the overlay reticle means that if we do 40 exposure sequences at a dose of Eo ~~each~~ <u>each;</u> the net effect is to expose the wafer with a dose of 2*Eo and to have effectively averaged over 20 or more exposures.

Please amend the paragraphs beginning on page 39, line 1, through page 42, line 6, as follows:

As a typical example, a production run at 4*Eo (a=4), using an overlay reticle that is 98% reflecting (R=0.98) and requiring a dose on the measurement wafers of 2*Eo (b=2) means the number of required exposures is (eq 31) ~~N=26~~ <u>N=26,</u> and the minimum number of exposures we are effectively averaging over for the purposes of reducing the random error component is (eq 32) Neff = 13 or greater. In this example, we could be averaging over as many as N=26 exposures, but this will <u>be</u> dependent on the specific resist and resist development sequence. Furthermore even though the exposure dose was set at the production dose (4*Eo) the dose at the wafer was sub-Eo (less than Eo) because it is equal to (1-R)*4*Eo = 0.08*Eo or 8% of Eo. We have described this embodiment with respect to a partially reflecting reticle. The considerations are similar if the overlay reticle is absorbing, as it would be for overlay groups made entirely as an attenuating phase shift mask *See* The Attenuated Phase Shift Mask, B. Lin instead of reflecting; all that is required is a reticle with a decreased optical transmission from normal. To be useful, the reticle

typically needs an optical transmission (1-R for a reflective mechanism) of < 50% of normal or nominal.

Reticle Plate

A portion of the reticle plate for the preferred embodiment is shown in Figure ~~21~~ 21A. The preferred embodiment makes no strict requirements on the size of the reticle plate, the shape of the overlay target patterns or the types of materials used to fabricate the mask plate. Hundreds of different overlay target patterns are available, some are shown in ~~*See*~~ US Patent 6,079,256, *supra*; Matching Management of Multiple Wafer Steppers Using a Stable Standard and a Matching Simulator, *supra*; Automated Electrical Measurements of Registration Errors in Step and Repeat Optical Lithography Systems, *supra*; US Patent 5,757,507, *supra*; US Patent 6,143,621, *supra*. The preferred embodiment will work with any stepper or scanner system using any type of overlay targets. The accuracy of the measurement technique does depend on the overlay sampling ~~density~~ density, and this should be considered. Heretofore, we have considered the reticle creating the overlay patterns as perfect. In practice errors in the reticle manufacture can be taken into account by first measuring the position of all the individual structures in all of the overlay groups using an absolute metrology tool such as the Nikon 5I. *See* Measuring System XY-5i, *supra* or Leica LMS IPRO; Leica LMS IPRO Brochure, *supra*. Next, in formulating equations 6-9, this reticle error (divided by the projection imaging tool demagnification, M) is explicitly written out on the right hand side and then subtracted from the resulting overlay measurements on the left hand side of the equations (thereby canceling out on the right hand side). The result is equations 6-9 as they are written above but with a correction applied to the overlay measurements appearing on the left hand side. The solution and further interpretation then proceeds word for word as before.

Further Embodiments

Instead of the reticle of Figure ~~21~~ 21A, this technique could be carried out with other reticle layouts, for example the reticle layout of Figure 41. It consists of an Mx X My array of alternating inner box labeled 1 in Figure 41 and shown in detail in Figure 42, and outer box labeled 2 in Figure 41 and shown detail in Figure 43, on regular pitch p*M. Inner box 1 and outer box 2 form are complementary to one another and so form a completed alignment attribute when overlaid on one another. So there is now only one overlay feature within each overlay group as opposed to the three overlay features per overlay group of Figure ~~21~~ 21A. A difference now is that the wafer stage displacements required to produce an interlocking pattern, such as shown in Figure 26 are odd integer multiples of the pitch, p illustrated in Figure 41. Put differently, the wafer stepping distance in X is set by the distance between the leftmost box in the row of a projected field and the furthest complementary box on the right edge of the projected field. An inner box is complimentary to an outer box and vice-versa. The distance between fields in the Y direction is similarly determined. The pitch of inner and outer box patterns on the reticle, see Figure 41, is p*M where M is the reduction magnification ratio of the projection lithography tool ~~(typically 4 or 5)~~ (typically 4 or 5), and p is the pitch of the features as projected onto the wafer.

A simple reticle with which this technique can be carried out is illustrated in Figure 45. It consists of two outer boxes (2) set along the left edge (first column) of the reticle and two inner boxes (1) set along the right edge (second column) with each inner box lying along the same row (same nominal y position) as an outer box along the left edge. The inner (1) and outer (2) boxes form a complementary pair of alignment attributes so that overlapping them forms a completed alignment attribute. Figure ~~8A~~ 8B shows one form for the outer box (2) on the reticle while Figure ~~10A~~ 10B shows one form for the inner box ~~(1)~~ (1), and the completed alignment attribute as exposed on an M=4 (4:1 reduction magnification system) is shown in Figure ~~12A~~ 12B.

In Figure ~~12A~~ 12B, the dark areas are unexposed resist so that in positive resist after the resist development process the dark area would correspond to remaining photoresist on the wafer while the white area would have no photoresist. In addition to the alignment attributes of the first and second column, there are 2 additional outer boxes (2) disposed along the bottom edge (first row) of the reticle. This first row is also located below, or in the negative y direction from the inner and outer boxes located in the first and second column and furthermore, the outer boxes in the first row are located at x positions in between the first and second columns and not on either of the first and second columns. This is so that the boxes in the first and second columns and the first row overlap with at most 1 other field when this reticle is exposed in an interlocking field stepping pattern. Along a second row which is above, or in the positive y direction from any of the before mentioned inner or outer boxes are two inner boxes (1) that are in the same columns or same x positions as the two outer boxes (2) along the first row. This pattern is minimal for the purposes of this invention in that only two interlocking exposures along each edge of a field can occur and there are no other redundant features.

Please amend the paragraphs beginning on page 43, line 3, through page 44, line 15, as follows:

The overlay metrology tool utilized by the present technique is typically a conventional optical overlay tool such as those manufactured by KLA-Tencor (*See* KLA 5105 Overlay Brochure, *supra*; KLA 5200 Overlay Brochure, *supra*) or Bio-Rad Semiconductor Systems. *See* Quaestor Q7 Brochure, Bio-rad Semiconductor Systems, *supra*. Other optical overlay tools that can be used by the present invention include those described in ~~See~~ US Patent 5,438,413, *supra*. In addition, some steppers or scanners (*See* Matching Management of Multiple Wafer Steppers Using a Stable Standard and a Matching Simulator, *supra*) can utilize their wafer alignment systems and wafer stages to function as overlay tools. However, in this role we would limit the total size of the alignment attribute (consisting of 2 wafer

alignment marks) to a distance over which the wafer stage would be as accurate as a conventional optical overlay tool. This distance is typically < 0.5 mm. When electrical alignment attributes are used for overlay (*See* Matching Management of Multiple Wafer Steppers Using a Stable Standard and a Matching Simulator, *supra*; Automated Electrical Measurements of Registration Errors in Step and Repeat Optical Lithography Systems, *supra*; US Patent 6,143,621, *supra*), the overlay metrology tool as utilized by this invention would correspond to the electrical equipment utilized for making the corresponding measurement.

The present invention has been mainly described with respect to ~~it's~~ its application on the projection imaging tools (steppers *See* Direct-referencing Automatic Two-points Reticle-to-Wafer Alignment Using a Projection Column Servo System, *supra*; New o.54 Aperature I-Line Wafer Stepper With Field by Field Leveling Combined with Global Alignment, *supra*; US Patent 4,861,146 Variable Focal Lens Device, *supra*), and scanners (*See* Micrascan(TM) III Performance of a Third Generation, Catadioptric Step and Scan Lithographic Tool, *supra*; ArF Step And Scan Exposure System For 0.15 Micron and 0.13 micron Technology Node, *supra*; 0.7 NA DUV Step and Scan System for 150nm Imaging with Improved Overlay, *supra*) most commonly used in semiconductor manufacturing today. The methods of the present invention can be applied to other projection imaging tools such as contact or proximity printers (*See* Optical Lithography Thirty Years and Three Orders of Magnitude, *supra*) 2-dimensional scanners, (*See* Large Area Fine Line Patterning By Scanning Projection Lithography, *supra;* US Patent 5,285,236, *supra*; Optical Lithography Thirty Years and Three Orders of Magnitude, *supra*), and next generation lithography (ngl) systems such as XUV (*See* Development of XUV Projection Lithography at 60-80 nm, *supra*), SCALPEL, EUV (Extreme Ultra Violet), (*See* Reduction Imaging at 14nm Using Multilayer-Coated Optics: Printing of Features Smaller than 0.1 Micron, J. Bjorkholm, et. al., Journal Vacuum Science and Technology, B8(6), 1509:1513, Nov/Dec 1990), x-ray imaging systems, IPL (Ion

Projection Lithography), and EPL (electron projection lithography). *See* Mix-And-Match: A Necessary Choice, *supra*.

Please amend the paragraph on page 45, lines 1-7, as follows:

So far, we have described the substrates on which the recording media is placed as wafers. This will be the case in semiconductor manufacture. The exact form of the substrate will be dictated by the projection lithography tool and ~~it's~~ its use in a specific manufacturing environment. Thus, in a flat panel manufacturing facility, the substrate on which the photoresist would be placed would be a glass plate or panel. A mask making tool would ~~utilized~~ utilize a reticle as a substrate. Circuit boards or multi-chip module carriers are other possible substrates.